VS-ST280C Series

Vishay Semiconductors



Phase Control Thyristors (Hockey PUK Version), 500 A



TO-200AB (A-PUK)

PRODUCT SUMMARY						
Package	TO-200AB (A-PUK)					
Diode variation	Single SCR					
I _{T(AV)}	500 A					
V _{DRM} /V _{RRM}	400 V, 600 V					
V _{TM}	1.36 V					
I _{GT}	90 mA					
TJ	-40 °C to 125 °C					

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS							
PARAMETER	TEST CONDITIONS	VALUES	UNITS				
1		500	A				
I _{T(AV)}	T _{hs}	55	°C				
1		960	А				
I _{T(RMS)}	T _{hs}	25	°C				
1	50 Hz	7850	Α				
I _{TSM}	60 Hz	8220					
l ² t	50 Hz	308	kA ² s				
1-1	60 Hz	281	- KA-5				
V _{DRM} /V _{RRM}		400 to 600	V				
tq	Typical	100	μs				
TJ		- 40 to 125	C°				

ELECTRICAL SPECIFICATIONS

VOLTAGE R	VOLTAGE RATINGS									
TYPE NUMBER	VOLTAGE CODE	V _{DRM} /V _{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM} MAXIMUM AT T_J = T_J MAXIMUM mA$						
ST280CC	04	400	500	30						
06		600	700							

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COMPLIANT

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ABSOLUTE MAXIMUM RATING	5					
PARAMETER	SYMBOL		TEST CON	IDITIONS	VALUES	UNITS
Maximum average on-state current	1	180° condu	ction, half sine v	wave	500 (185)	А
at heatsink temperature	I _{T(AV)}	double side	(single side) coo	bled	55 (85)	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C	heatsink temp	erature double side cooled	960	
		t = 10 ms	No voltage		7850	
Maximum peak, one-cycle		t = 8.3 ms	reapplied		8220	A kA ² s
non-repetitive surge current	I _{TSM}	t = 10 ms	100 % V _{RRM}		6600	
		t = 8.3 ms	reapplied	Sinusoidal half wave, initial T _J = T _J maximum	6900	
Martin and Participation		t = 10 ms	No voltage reapplied		308	
	l ² t	t = 8.3 ms			281	
Maximum I ² t for fusing	1-1	t = 10 ms	100 % V _{RRM}		218	
		t = 8.3 ms	reapplied		200	
Maximum I ² \sqrt{t} for fusing	l²√t	t = 0.1 to 10) ms, no voltage	reapplied	3080	kA²√s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % x π	$x _{T(AV)} < l < \pi x$	$I_{T(AV)}$), $T_J = T_J$ maximum	0.84	v
High level value of threshold voltage	V _{T(TO)2}	$(I > \pi \times I_{T(AV)})$), $T_J = T_J$ maxin	num	0.88	v
Low level value of on-state slope resistance	r _{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T _J = T _J maximum			0.50	mΩ
High level value of on-state slope resistance	r _{t2}	$(I > \pi x I_{T(AV)}), T_J = T_J maximum$			0.47	1115.2
Maximum on-state voltage	V _{TM}	I _{pk} = 1050 A	λ, T _J = 125 °C, t	_p = 10 ms sine pulse	1.36	V
Maximum holding current	Ι _Η	T _ 05 °C	anada aunrhi 1	2. V registive lead	600	m۸
Maximum (typical) latching current	١L	$1_{\rm J} = 25$ C,	anoue supply 1	2 V resistive load	1000 (300)	mA

SWITCHING							
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Maximum non-repetitive rate of rise of turned-on current	dl/dt	Gate drive 20 V, 20 $\Omega, t_r \leq$ 1 μs T_J = T_J maximum, anode voltage \leq 80 % V_{DRM}	1000	A/µs			
Typical delay time	t _d	Gate current 1 A, dl _g /dt = 1 A/ μ s V _d = 0.67 % V _{DRM} , T _J = 25 °C	1.0				
Typical turn-off time	t _q	I_{TM} = 300 A, T_J = T_J maximum, dl/dt = 20 A/µs, V_R = 50 V, dV/dt = 20 V/µs, gate 0 V 100 $\Omega,$ t_p = 500 µs	100	μs			

BLOCKING							
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs			
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA			



TRIGGERING							
PARAMETER	SYMBOL	OL TEST CONDITIONS		VAL	UNITS		
FARAMETER	STINDUL		TEST CONDITIONS		MAX.		
Maximum peak gate power	P _{GM}	T _J = T _J maximum,	t _p ≤ 5 ms	10).0	w	
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum,	f = 50 Hz, d% = 50	2	.0	vv	
Maximum peak positive gate current	I _{GM}	$T_J = T_J$ maximum,	$t_p \le 5 \text{ ms}$	3	.0	А	
Maximum peak positive gate voltage	+ V _{GM}		t < 5 mg	20		- V	
Maximum peak negative gate voltage	- V _{GM}	ij = ij maximum,	$_{\rm J}$ maximum, $t_{\rm p} \le 5$ ms 5.0		.0		
		T _J = - 40 °C	- -	180	-		
DC gate current required to trigger	I _{GT}	T _J = 25 °C		90	150	mA	
		T _J = 125 °C	$T_J = 125 \text{ °C}$ Maximum required gate trigger/ current/voltage are the lowest		-		
		T _J = - 40 °C	value which will trigger all units 12 V anode to cathode applied	2.9	-		
DC gate voltage required to trigger	V _{GT}	T _J = 25 °C	12 V anoue to cathode applied	1.8	3.0	V	
		T _J = 125 °C	J = 125 °C		-		
DC gate current not to trigger	I _{GD}		Maximum gate current/voltage not to trigger is the maximum	10		mA	
DC gate voltage not to trigger	V _{GD}	$T_J = T_J maximum$	value which will not trigger any unit with rated V _{DRM} anode to cathode applied	0.30		v	

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum operating junction temperature range	TJ		- 40 to 125	°C		
Maximum storage temperature range	T _{Stg}		- 40 to 150			
Maximum thermal resistance,	D	DC operation single side cooled	0.17			
junction to heatsink	R _{thJ-hs}	DC operation double side cooled	0.08	K/W		
Maximum thermal resistance,	Р	DC operation single side cooled	0.033	- r./ vv		
case to heatsink	R _{thC-hs}	DC operation double side cooled	0.017			
Mounting force, ± 10 %			4900 (500)	N (kg)		
Approximate weight			50	g		
Case style		See dimensions - link at the end of datasheet	TO-200AB (A-F	PUK)		

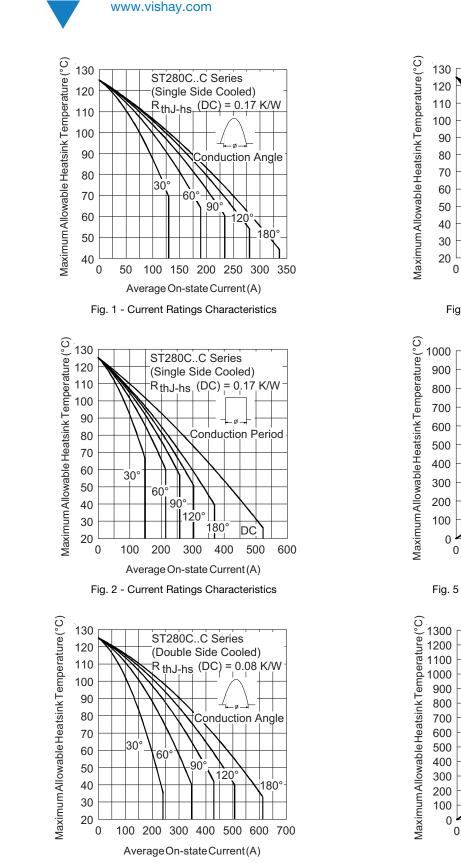
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR	R CONDUCTION	TEST CONDITIONS			
CONDUCTION ANGLE	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE	TEST CONDITIONS	UNITS		
180°	0.016	0.016	0.011	0.011				
120°	0.019	0.019	0.019	0.019				
90°	0.024	0.024	0.026	0.026	$T_J = T_J maximum$	K/W		
60°	0.035	0.035	0.036	0.037				
30°	0.060	0.060	0.060	0.061				

Note

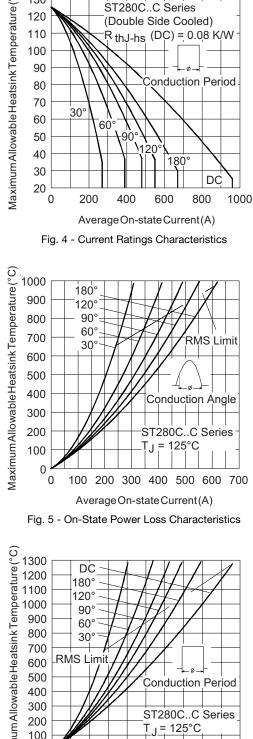
• The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

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Average On-state Current(A) Fig. 6 - On-State Power Loss Characteristics

600

800

400

200

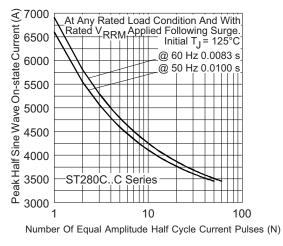
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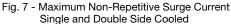
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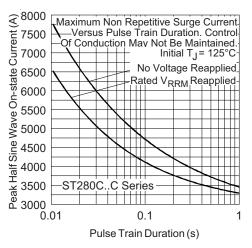
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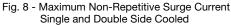
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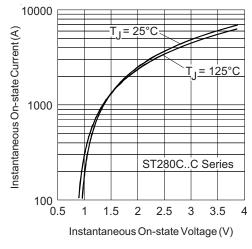
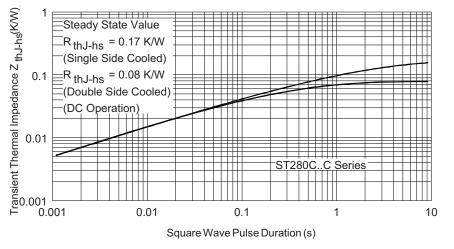


Fig. 9 - On-State Voltage Drop Characteristics





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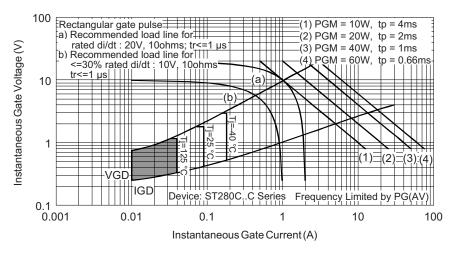


Fig. 11 - Gate Charactersitics

ORDERING INFORMATION TABLE

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Device code	VS-	ST 28	0	С	06	С	1	-	
	1	2 3	4	5	6	7	8	9	
	1 - 2 -	Vishay Ser Thyristor	niconduo	ctors pro	oduct				
	3 -	Essential p							
	4 - 5 -	0 = Conver C = Ceram	0	9					
	6 -	-				-	Itage Ra	atings table)	
	7 - 8 -	C = PUK c					thode u	nsoldered lea	de)
	o -	-				-		unsoldered lea	
				.0		,		oldered leads	,
		3 = Fast-or	termina	ls (gate	and au	xiliary c	athode	soldered lead	s)
	9 -	Critical dV/				(standar ecial se		-	

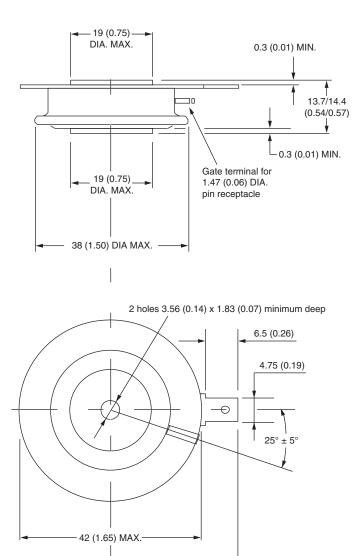
LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95074			



TO-200AB (A-PUK)

DIMENSIONS in millimeters (inches)

Anode to gate Creepage distance: 7.62 (0.30) minimum Strike distance: 7.12 (0.28) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)

28 (1.10)



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