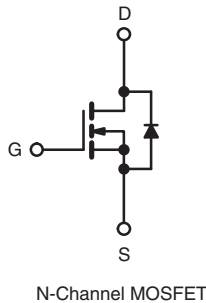
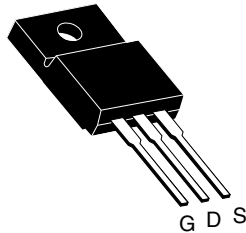


## S Series Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ at $T_J$ max. (V)	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.190
$Q_g$ max. (nC)	98	
$Q_{gs}$ (nC)	17	
$Q_{gd}$ (nC)	25	
Configuration	Single	

**TO-220 FULLPAK**


### FEATURES

- Generation one
- High  $E_{AR}$  capability
- Lower figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- Ultra low  $R_{on}$
- $dV/dt$  ruggedness
- Ultra low gate charge ( $Q_g$ )
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### APPLICATIONS

- PFC power supply stages
- Hard switching topologies
- Solar inverters
- UPS
- Motor control
- Lighting
- Server telecom


ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF22N60S-E3

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	22	A
		$T_C = 100$ °C	13	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	65		
Linear Derating Factor		2	W/°C	
Single Pulse Avalanche Energy <sup>c</sup>	$E_{AS}$	690	mJ	
Repetitive Avalanche Energy <sup>b</sup>	$E_{AR}$	25		
Maximum Power Dissipation	$P_D$	250	W	
Drain-Source Voltage Slope	$dV/dt$	$T_J = 125$ °C	37	V/ns
Reverse Diode $dV/dt$ <sup>e</sup>			5.3	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s	300		

### Notes

- Limited by maximum junction temperature.
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.4	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	5	$\mu\text{A}$
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}$	-	0.160	0.190	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 13\text{ A}$		-	9.4	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$		-	2810	-	pF
Output Capacitance	$C_{oss}$			-	1480	-	
Reverse Transfer Capacitance	$C_{rss}$			-	33	-	
Effective Output Capacitance (Time Related)	$C_{oss\text{ eff.}}(TR)^a$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	155	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 22\text{ A}, V_{DS} = 480\text{ V}$	-	75	110	nC
Gate-Source Charge	$Q_{gs}$			-	17	-	
Gate-Drain Charge	$Q_{gd}$			-	25	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 380\text{ V}, I_D = 22\text{ A},$ $R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$		-	24	50	ns
Rise Time	$t_r$			-	68	100	
Turn-Off Delay Time	$t_{d(off)}$			-	77	115	
Fall Time	$t_f$			-	59	90	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{ open drain}$		-	0.65	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	22	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	88	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 22\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S,$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	462	690	ns
Reverse Recovery Charge	$Q_{rr}$			-	8.3	16	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	30	60	A

**Note**

a.  $C_{oss\text{ eff.}}(TR)$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

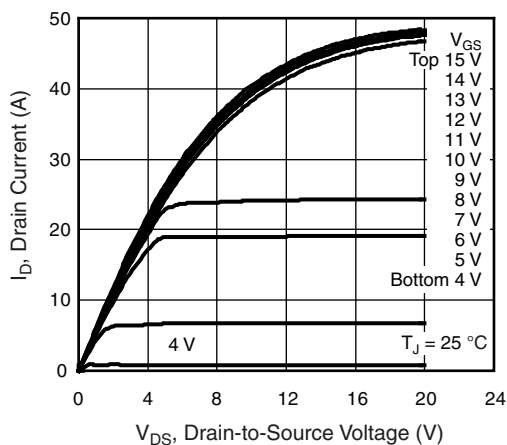


Fig. 1 - Typical Output Characteristics,  $T_J = 25\text{ }^\circ\text{C}$

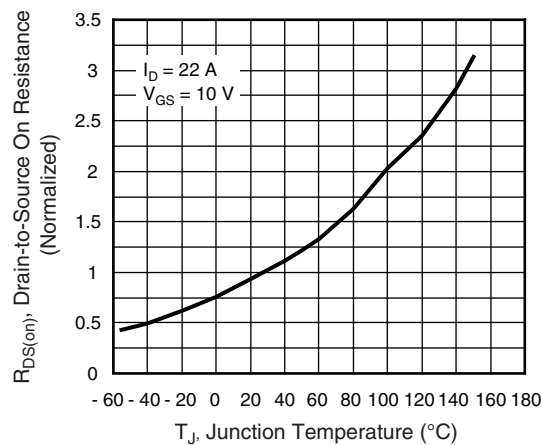


Fig. 4 - Normalized On-Resistance vs. Temperature

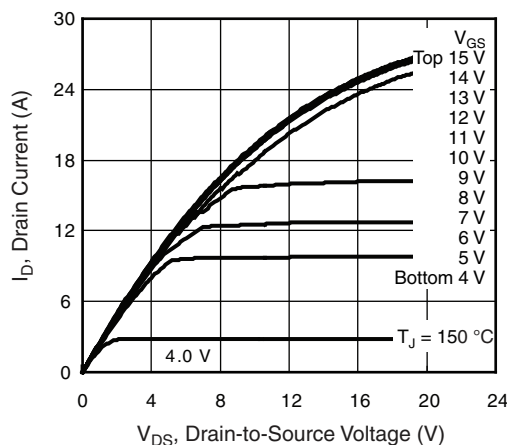


Fig. 2 - Typical Output Characteristics,  $T_J = 150\text{ }^\circ\text{C}$

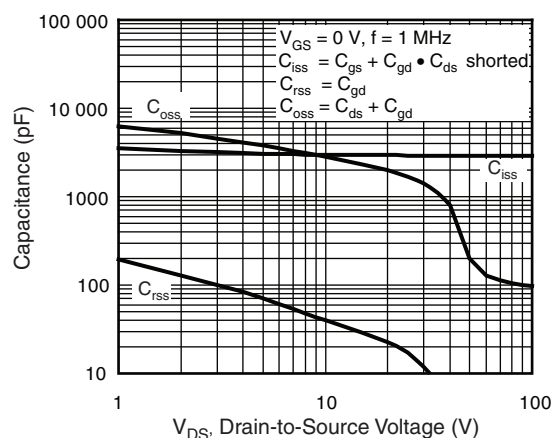


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

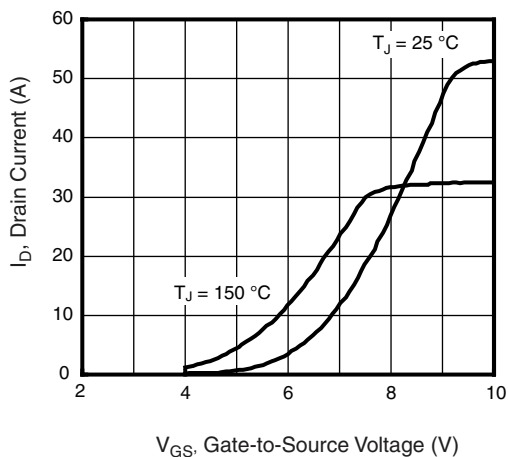


Fig. 3 - Typical Transfer Characteristics

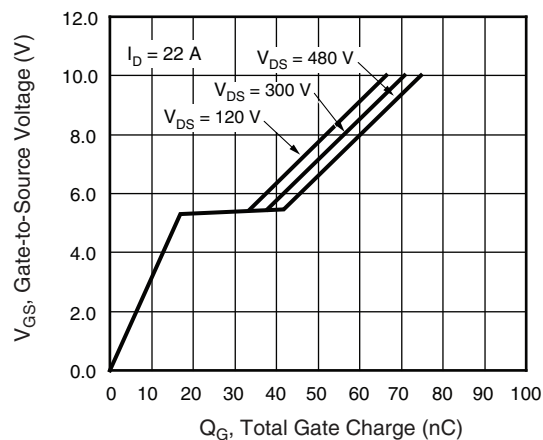
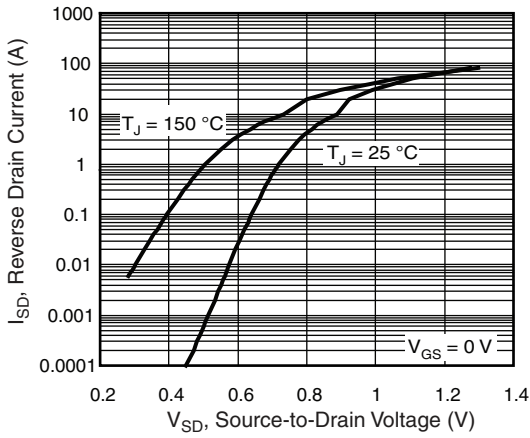
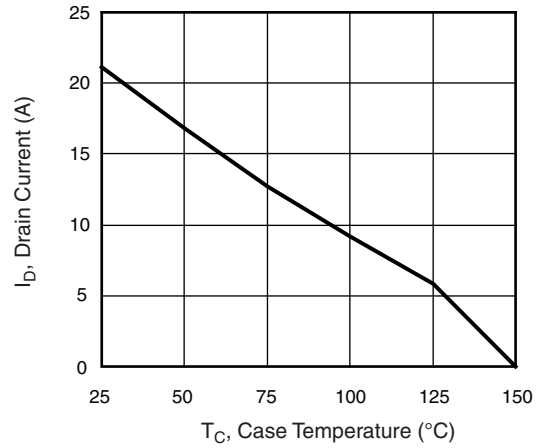


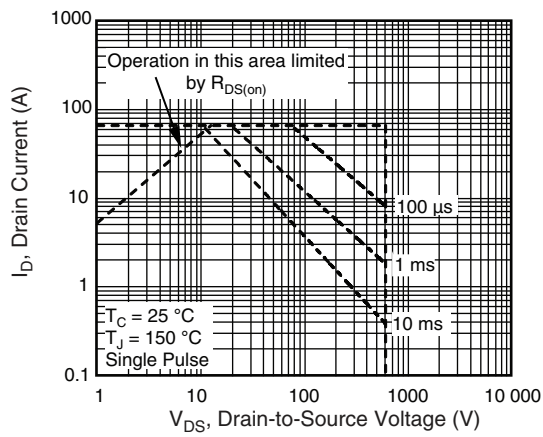
Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



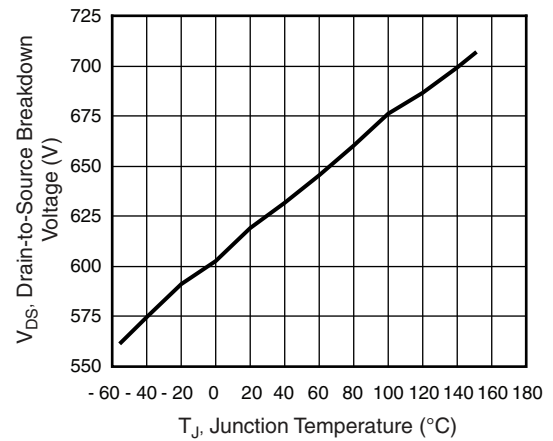
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



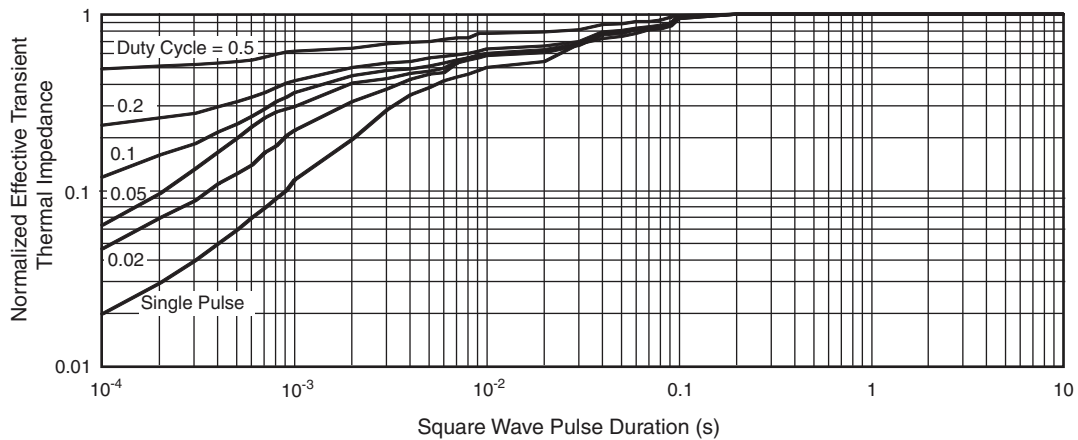
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Maximum Safe Operating Area**



**Fig. 10 - Drain-to-Source Breakdown Voltage**



**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**

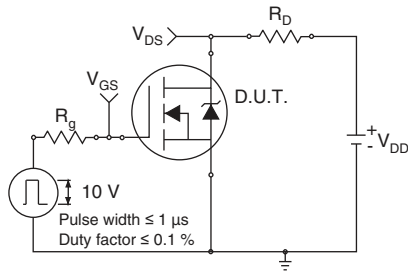


Fig. 12 - Switching Time Test Circuit

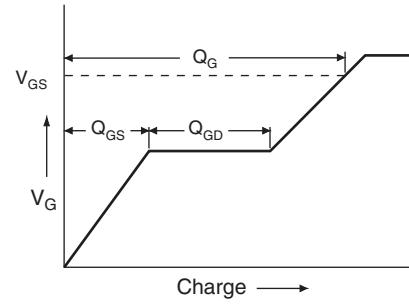


Fig. 16 - Basic Gate Charge Waveform

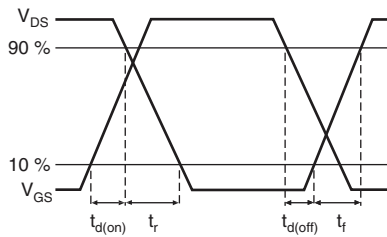


Fig. 13 - Switching Time Waveforms

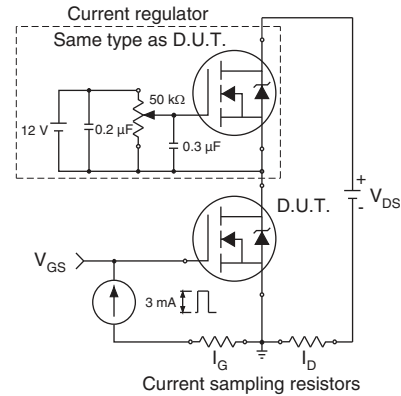


Fig. 17 - Gate Charge Test Circuit

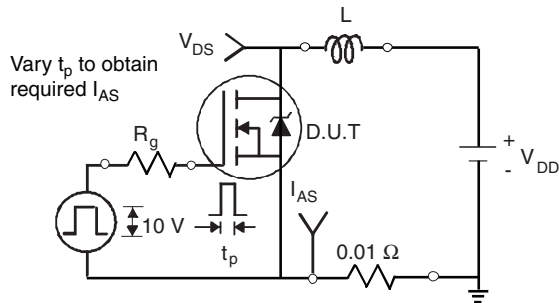


Fig. 14 - Unclamped Inductive Test Circuit

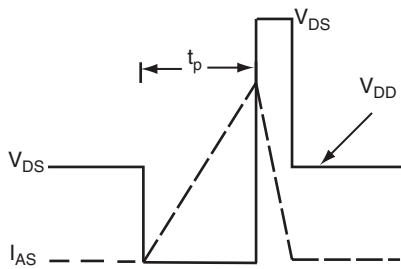
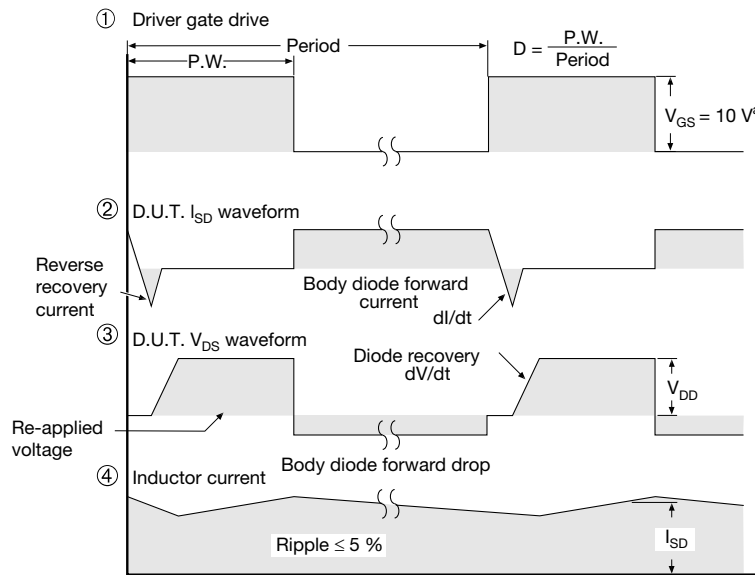
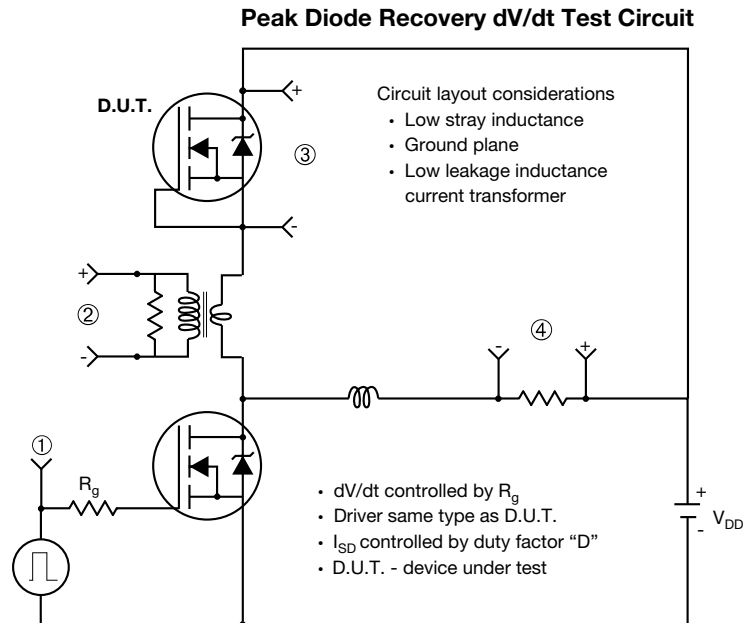


Fig. 15 - Unclamped Inductive Waveforms



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

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